Data Acquisition improvements at ISOLDE: first ideas

ISCC meeting 31.01.2012

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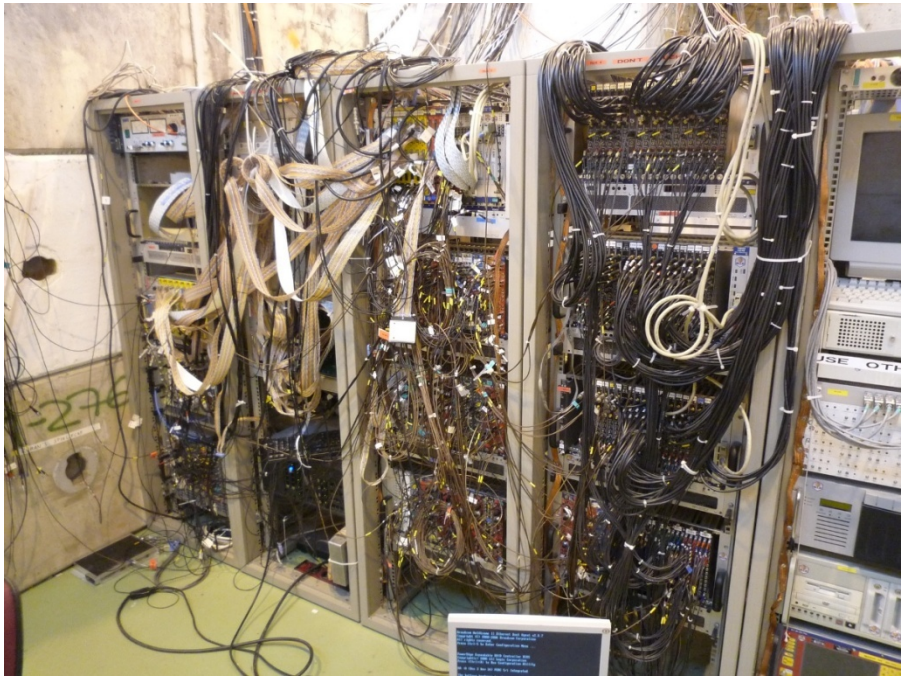
ISOLDE DAQ systems - overview

Different DAQ solutions available for ISOLDE experiments

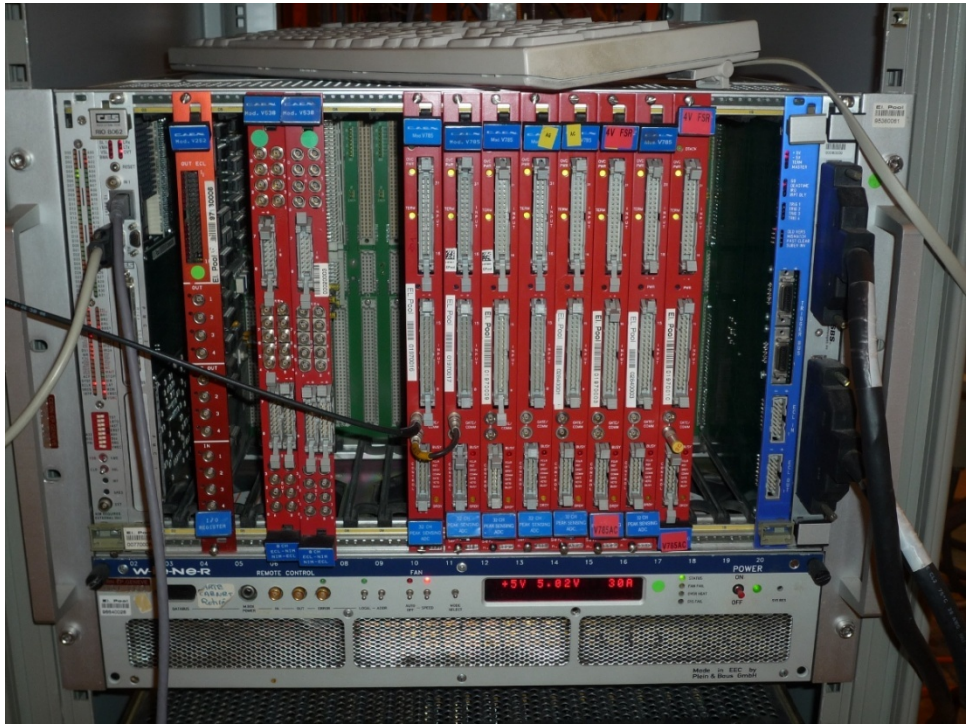
- Standard VME-based systems
- XIA-DGF4C + mb_collector software (Miniball, Nicole, ISOLTRAP, CRIS…)
- other (Digital oscilloscope, MCA…)



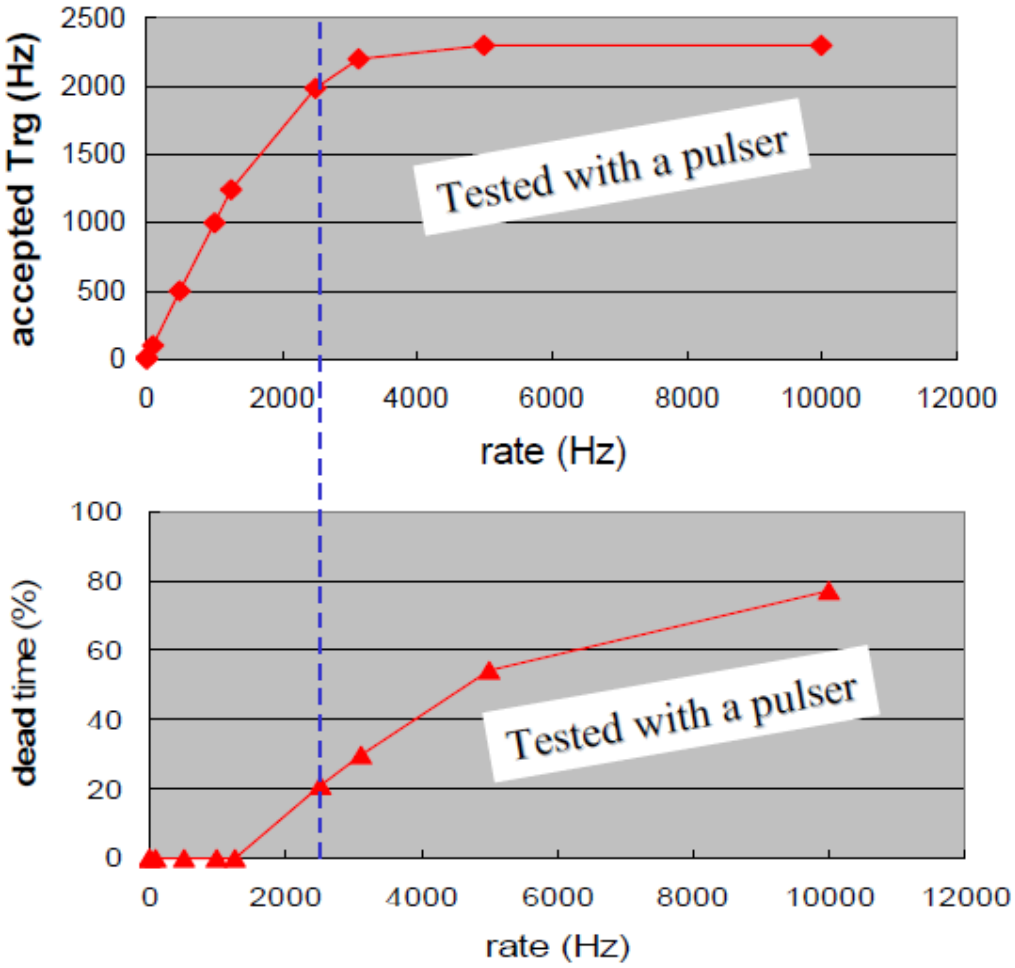
ISOLDE DAQ systems - MBS

Standard VME-based system

- The software is based on the MBS acquisition system from GSI (N. Kurz et al.).
- CES RIO2 processor
- The system comprises a set of CAEN V775/V785 TDCs and peak sensing ADCs
- TRIVA trigger synchronization module
- Well established within collaboration



MBS – single event mode (example)



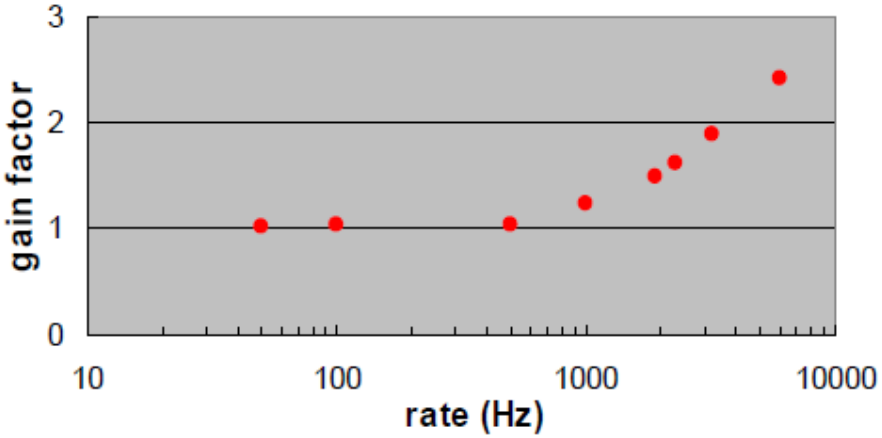
C. Nociforo et al.

The data sender is a RIO-3 CES (800MHz) processor which is located in the FRS VME crate. In this particular case, each event (i.e. VME ADC, TDC, QDC signals) is read out at each accepted trigger as 34 words. During this period, typically 120 µs, the DAQ is busy and any other trigger is rejected.

MBS – multi event mode

FRS multi-event DAQ tested with real particle rate and compared to single-event one:

- runs in stable condition
- more effective starting from 400 Hz
- gain factor = 2 at 4 kHz
- dead time at 10 kHz : 48%



C. Nociforo, N. Kurz, GSI report (2009)

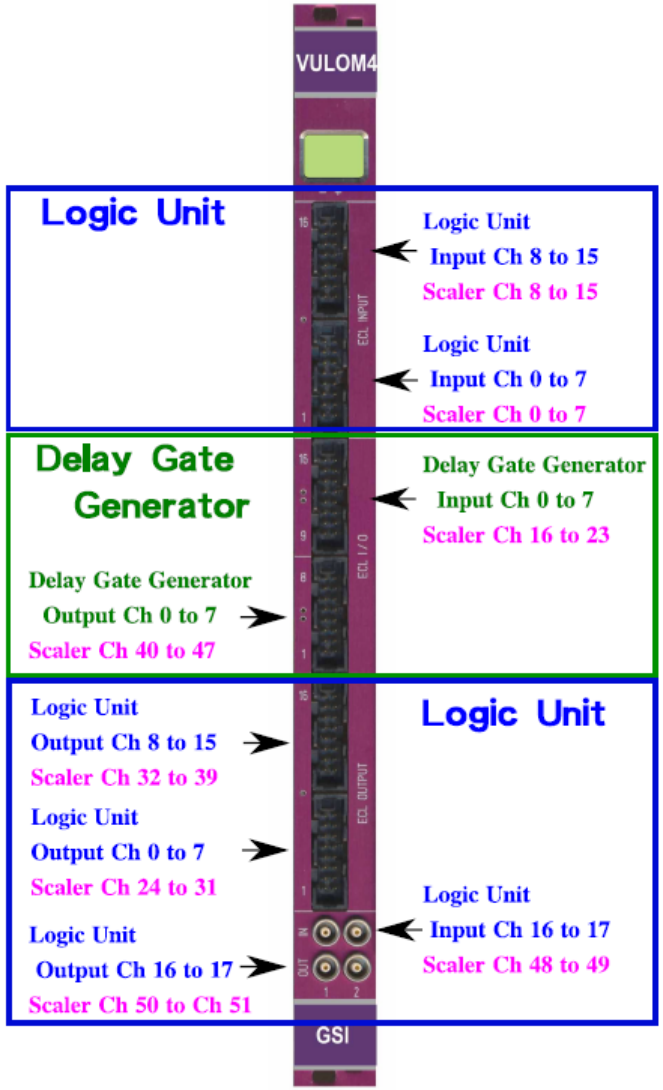
more efficient read out in BLock Transfer mode (BLT), which is supported by the VME Caen modules. A BLT read out of 32x34 words takes place and allows to read all events stored in the buffer (multi event mode).

VULOM – VME Universal Logic Module

•VULOM (VME Universal Logic Module) - 1-unit-wide VME 6U module with 16 ECL-inputs, 16 ECL-outputs, 16 ECLI/Os, 2 NIM-inputs and 2 NIM-outputs on its front-panel and a FPGA (Virtex 4 by Xilinx corp.)
•The logic to be loaded to the FPGA can be easily replaced via VME access - possible to use VULOM for various different purposes replacing many analogue modules

• An 18-input 18-output logic unit combined with clock generators.
• An 8-channel delay and gate generator.
• A scaler for 26 inputs and 26 outputs.

The logic unit with clock generators can produce OR or AND signals of inputs with enable, disable and inverse for both inputs and outputs, and clock signals by internal clock of the FPGA with frequency of 1 Hz-10 MHz.



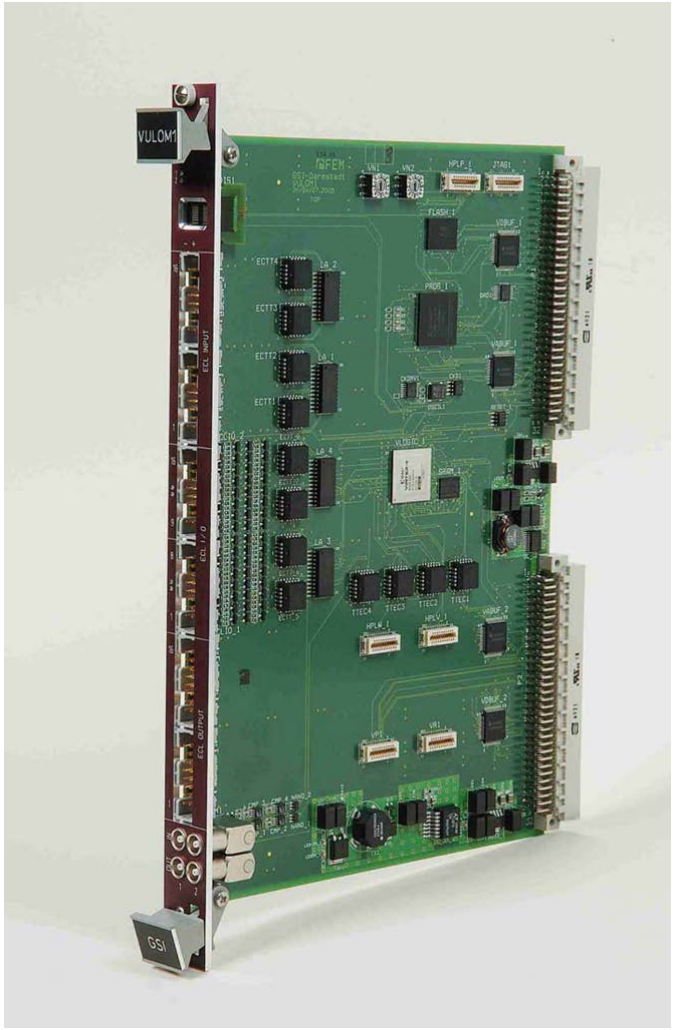
http://wiki.gsi.de/pub/Personalpages/ManualElectronics/vulom_univ_logic_v1.0.pdf

VULOM trigger electronics

Logic Matrix Unit

LMU setup Bit patterns Output

LMU Setup (1 to 16)	valid Input example	Output (1 to 16)
XXXXXXXXXXX+X+XX	0101101111011110	1000000000000000
-XXXXX+XXXXXX+XX	0000111000011111	0100000000000000
-XXXXXXXXXXX+XX	0100101101011111	0010000000000000
-XXXXX+XXXXXX+XX	0100111010111111	0001000000000000
X-XXXXXXXXXX+XX+	1000111010111111	0000100000000000
XXXXX+XXXXXX+XX+	1001111010111001	0000010000000000
+-+XXX+XXXXXX+XX	1010111101011111	0000001000000000
+--XXX+XXXXXX+X-	1000111101011110	0000000100000000
XXXXXXXX++XXX+XX	0100111111011111	0000000010000000
-XXXXX++XXXXXXX+	0100111110101111	0000000001000000
-XX-XX+X+XXXXXX+	0110111110101111	0000000000100000
-XX-XX+XX+XXXXX+	0100111101101111	0000000000010000
-XX-XX+XXX+XXXX+	0110111101010111	0000000000001000
-XX-XX+XXXX+XXX+	0010111101110011	0000000000000100
-XX-XX+XXXXX+XX+	0000111101011111	0000000000000010
-XX-XX+XXXXXX+X+	0110111100011101	0000000000000001



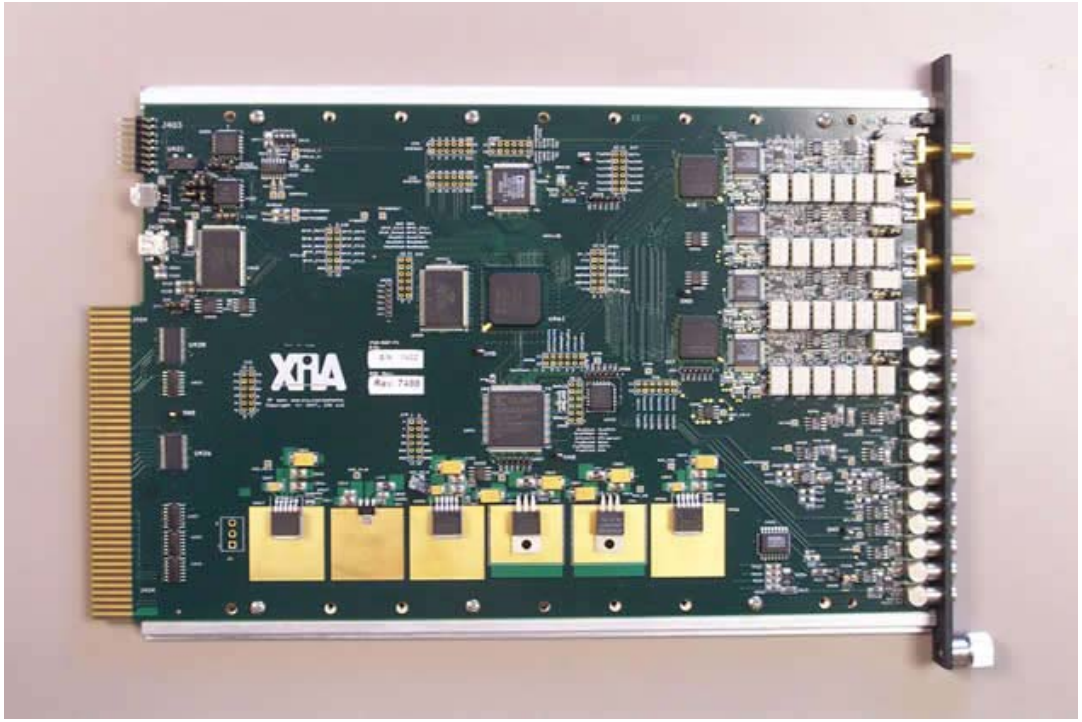
http://www.gsi.de/informationen/wti/ee/elekt_entwicklung/trigger_detailed.pdf

Digital Pulse Processing - alternatives

Digital Pulse Processing electronics (CAEN)

- V1724 14 bit 100 MS/s ADC, 8 channels
- FPGA for real time Digital Pulse Processing:
  - Pulse Height Analysis (DPP-PHA)
  - Zero Suppression (Standard Firmware)
- 2.25 Vpp input range (single ended or differential); single ended 500 mVpp & 10 Vpp also available – but **no** adjustable gain
- 16-bit programmable DC offset adjustment: ±1.125 V (±0.25 V / 5 V)
- Trigger Time stamps
- Memory buffer: 512 kS/ch or 4 MS/ch, up to 1024 events
- Programmable event size and pre-post trigger adjustment
- Analog Sum/Majority and digital over/under threshold flags for Global Trigger logic
- Front panel clock In/Out available for multiboard synchronisation (direct feed through or PLL based synthesis)
- Can be handled by MBS
- High hardwired threshold value – can be a problem for low energy X and gammas

DGF4C

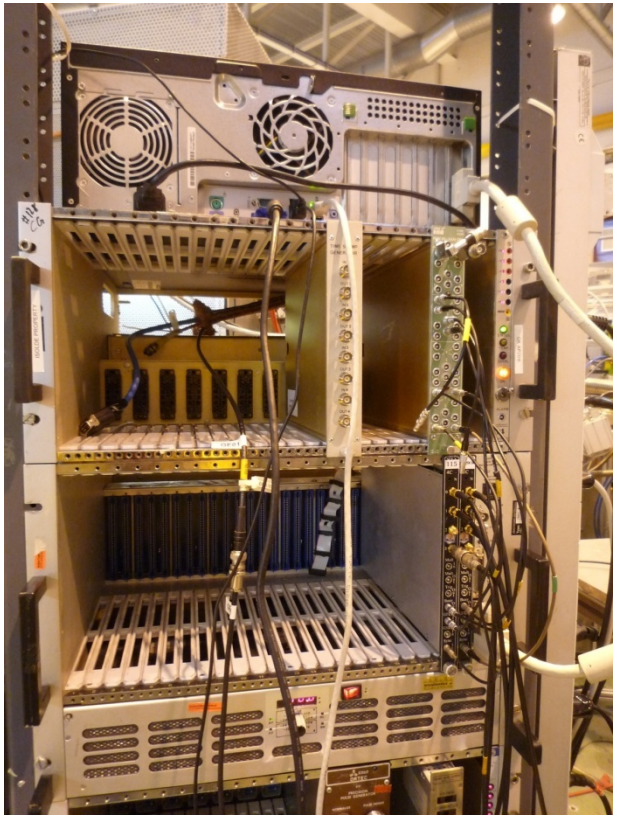


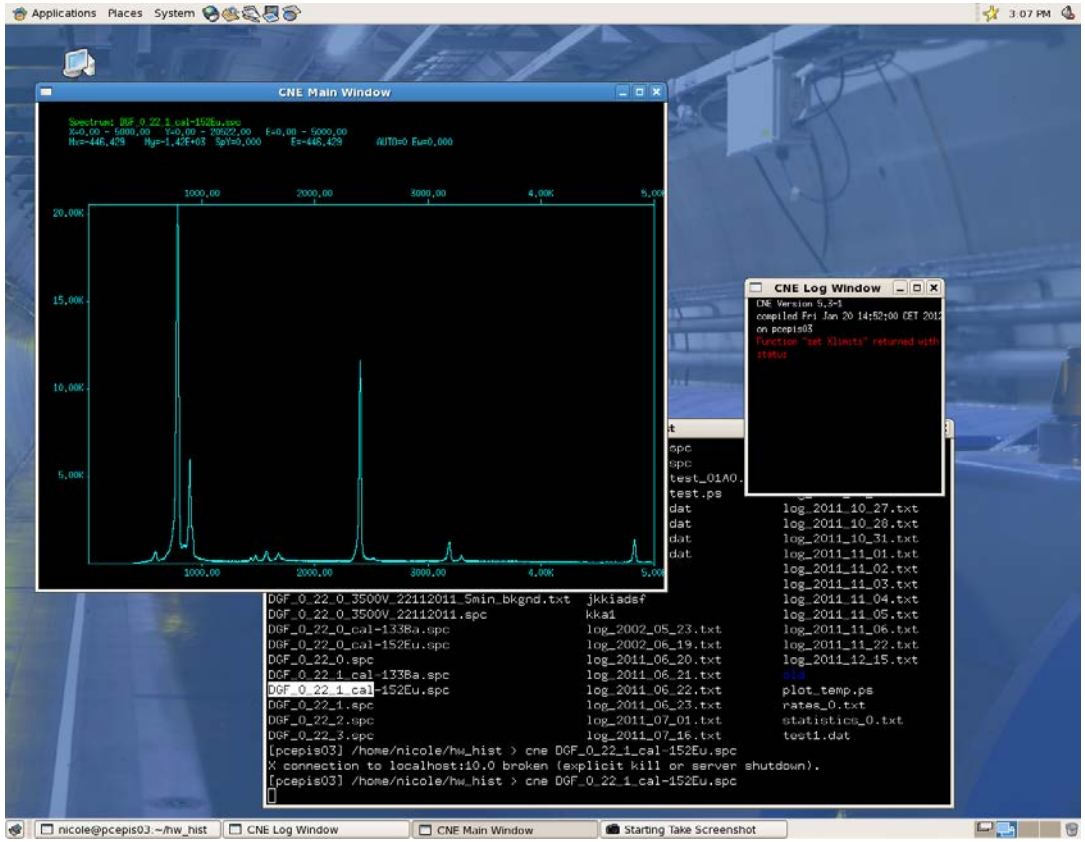
- Digital Gamma Finder (DGF) is a pulse processor with capabilities for measuring both energy and pulse shape
- Common clock distribution
- Above input rate of 5 kHz dead-time significant dead-time
- 40 MHz sampling rate (rev. D, E) → 80 MHz (rev. F). Upgrade presently being done.

DGF4C - DAQ system

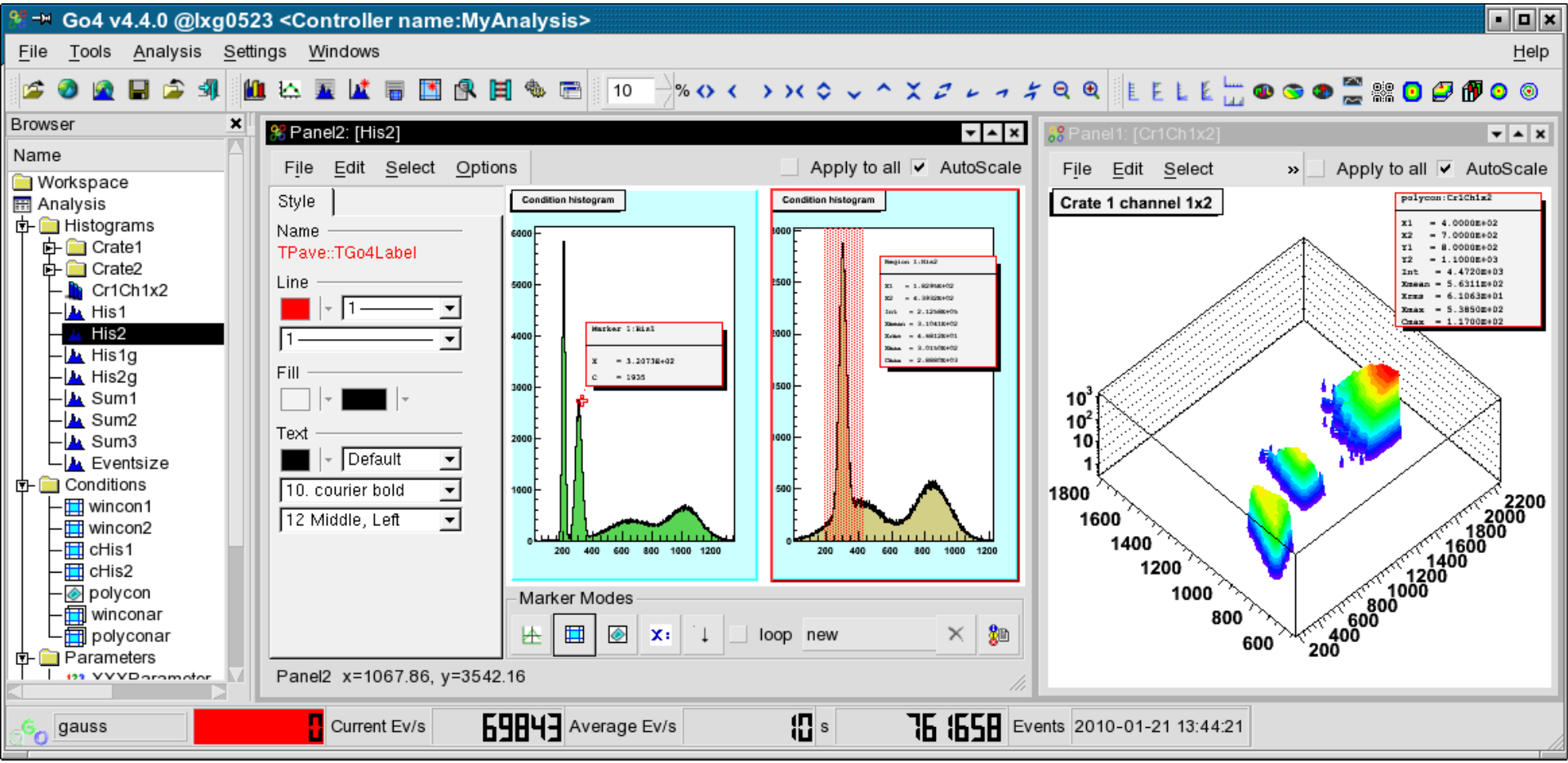
XIA DGF4c-based system (CRIS, ISOLTRAP, MB, NICOLE, others)

- Based on MB collector code (N. Warr, G. Simpson)
- Online monitoring using cne software
- Offline analysis by ROOT is also available.





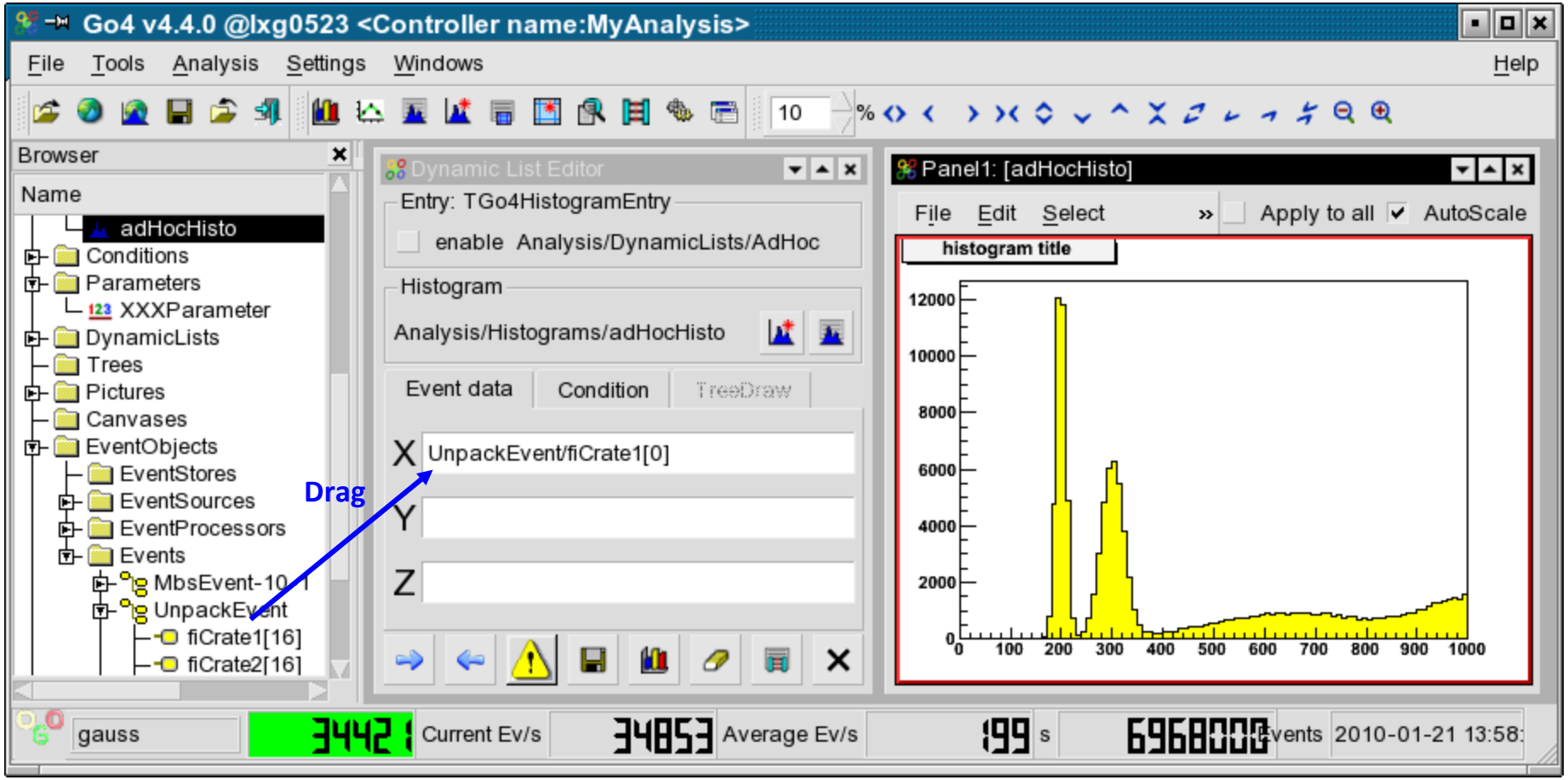
GO4 - View panel



- Graphical ROOT editor
- Show same histogram in different views (ranges, line and fill colors)
- Improved marker editor, may also edit conditions
- Info on time/date and full object path

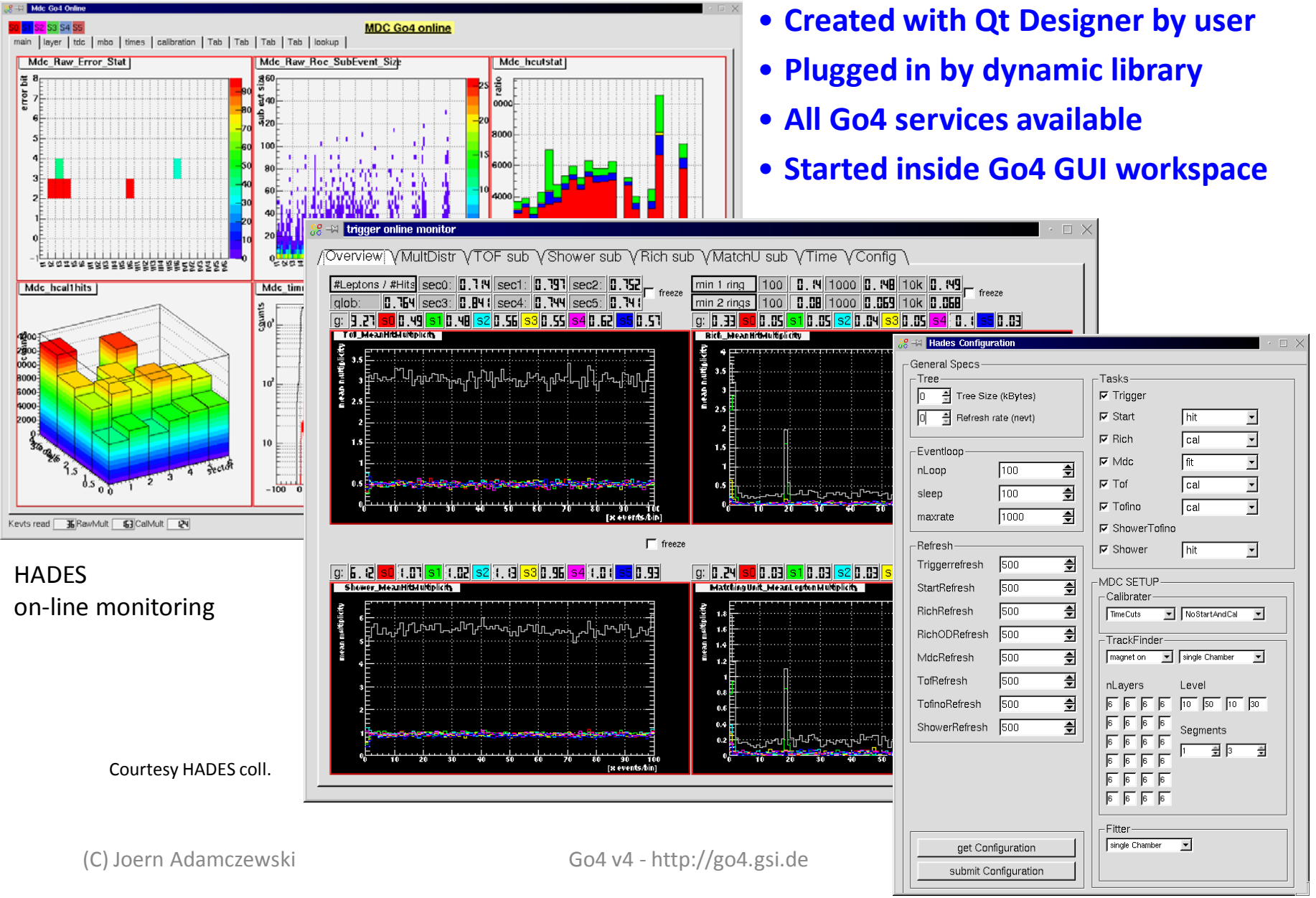
GO4 – Dynamic list editor

Histograming “ad hoc” from event data



GO4 – User GUI (Qt)

- **Created with Qt Designer by user**
- **Plugged in by dynamic library**
- **All Go4 services available**
- **Started inside Go4 GUI workspace**

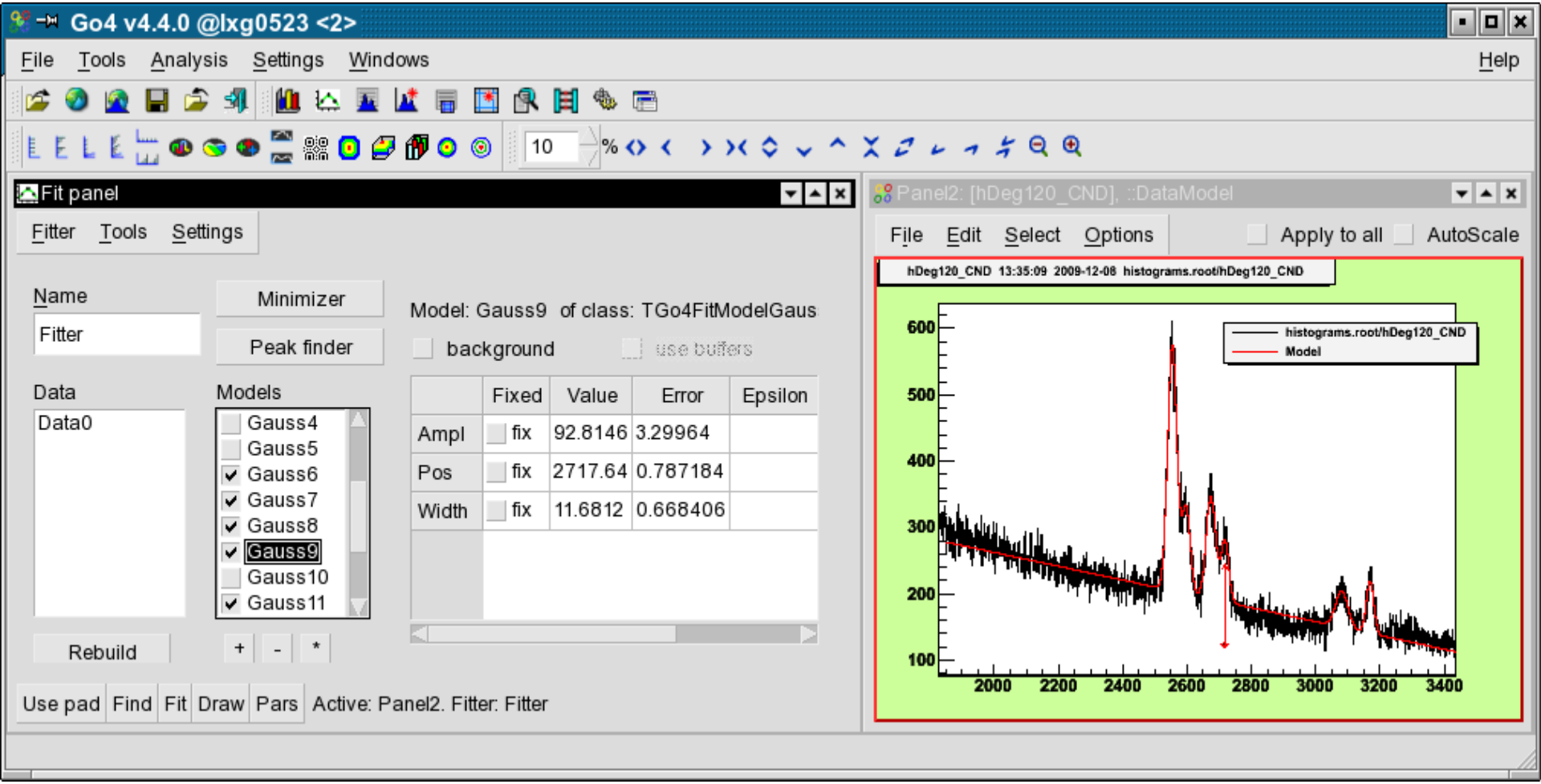


HADES
on-line monitoring

Courtesy HADES coll.

GO4 – Fit panel

Interactive peak finding and fitting. Save fitter for use in macros



DABC – Data Acquisition Backbone Core

- High speed network event building system for FAIR

- Test bed for the full readout chain from detectors, digitizers, readout controllers, data combiners to event building, filtering, and archiving.

- Self-triggered front-end systems with a very precise time distribution system.

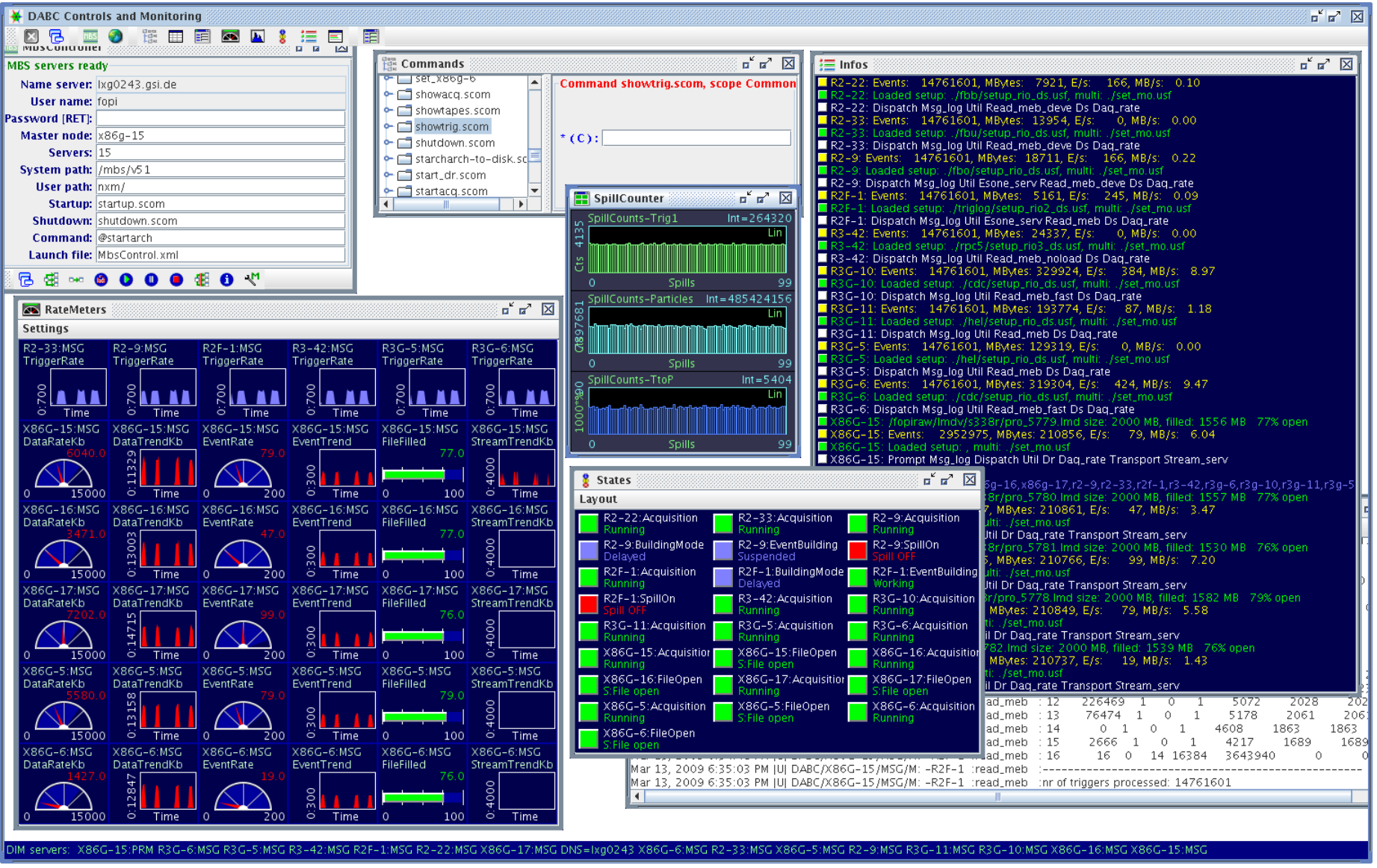
- Sorting of the data over the network will probably be not based on events, but rather on data packets of time slices. Only after the composition of these time slice fragments at the receiver nodes of the network an event definition will be possible.

- After that event data can be processed for filtering, compression, on-line analysis and storage. This processing might need large processing farms able to handle high data flows.

- Compatibility with existing DAQ (MBS)

http://dabc.gsi.de

DABC – controlling MBS



http://dabc.gsi.de/dabc/doc/CHEP09-S-09-00079.pdf

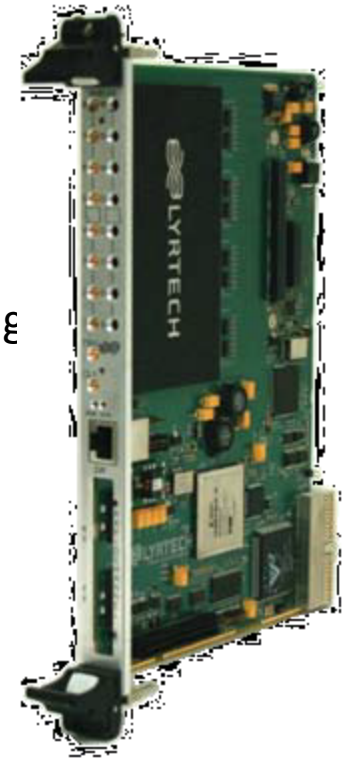
GRAIN

Grain is a data analysis framework developed at JYU to be used with the novel Total Data Readout (TDR) data acquisition system.

TDR based on Lyrtech VHS-ADC (Virtex IV FPGA) modules - sampling rate 105 MHz, 8ch 14bit, capable to handle rates ~30kHz/ch (DC beam).

In Total Data Readout all the electronics channels are read out asynchronously in singles mode and each data item is timestamped. Event building analysis has to be done entirely in the software post-processing the data stream.

A flexible and efficient event parser and the accompanying software framework written entirely in Java.

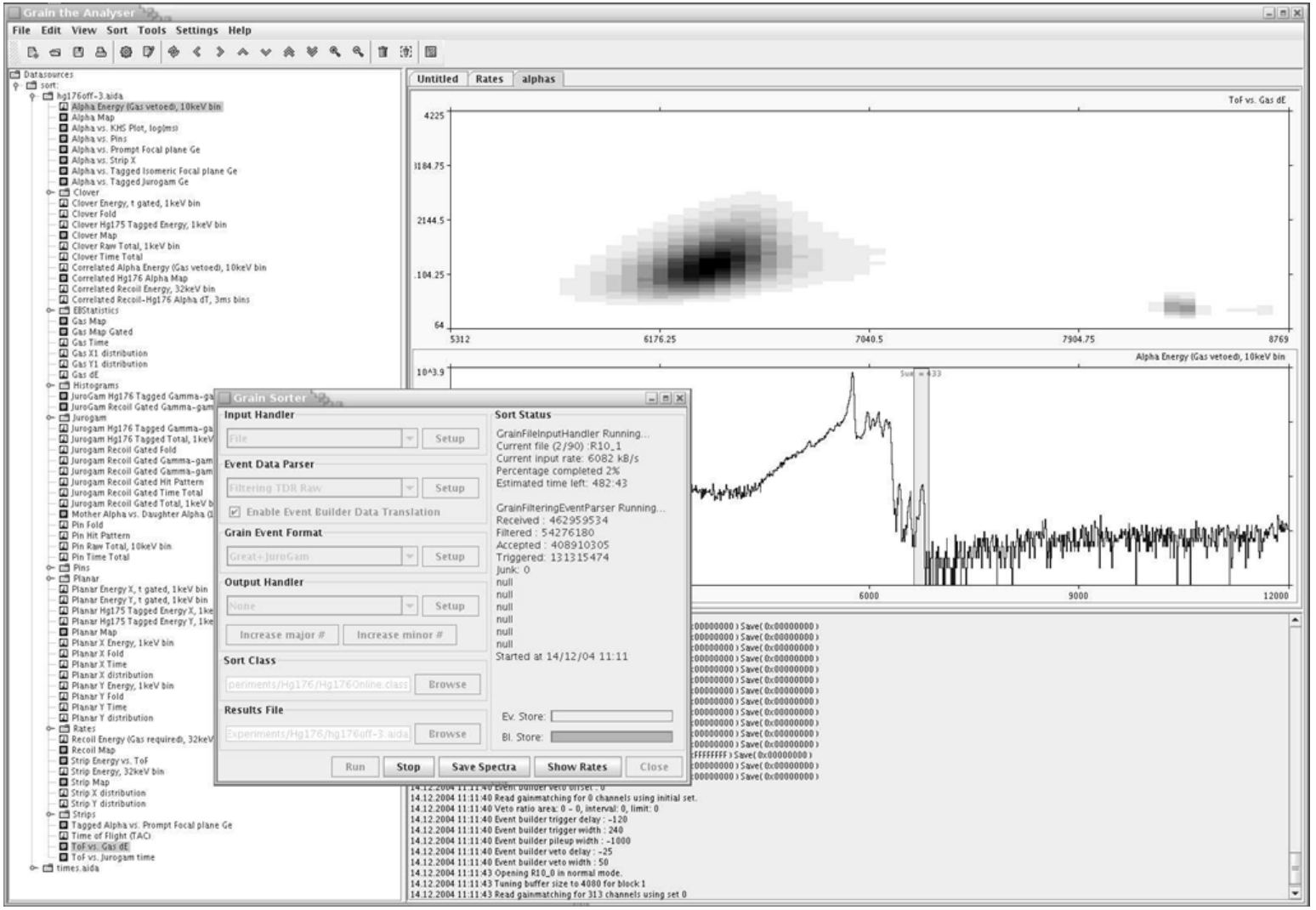


P. Rahkila, Grain - A Java Data Analysis System for Total Data Readout Nucl. Instr. and Meth. A 595, 637 (2008)

Grain

https://trac.cc.jyu.fi/projects/grain

GRAIN



Grain

https://trac.cc.jyu.fi/projects/grain

Summary

- Different solutions possible (hardware/software)

- Main problems reported by the community:
  - rate handling capability
  - DAQ/analysis GUI

- DAQ for low rate experiments requires smaller changes

This work is supported by ENSAR